National Semiconductor

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PC16450C/NS16450, PC8250A/INS8250A Universal Asynchronous Receiver/Transmitter

General Description

This part functions as a serial data input/output interface in a microcomputer system. The system software determines the functional configuration of the UART via a TRI-STATE® 8-bit bidirectional data bus.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The UART includes a complete MODEM-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

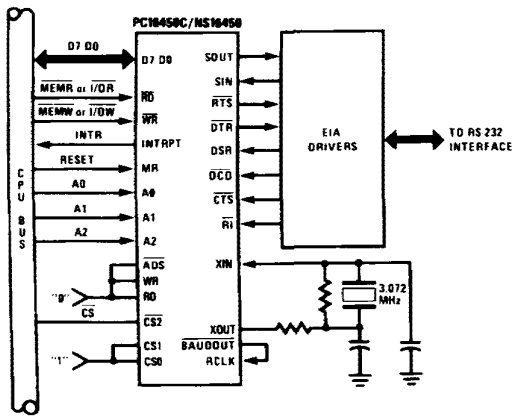
The PC16450C/NS16450 is an improved specification version of the PC8250C/INS8250-B Universal Asynchronous Receiver/Transmitter (UART). The UART is fabricated using National Semiconductor's advanced 1.25 μ CMOS process.

The PC16450C/NS16450 is functionally equivalent to the original NS16450, INS8250A, NS16C450 and INS82C50A, except that it has improved AC timing specifications and it is CMOS.

Features

- Easily interfaces to most popular microprocessors.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.
- Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16 × clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 256 kbaud)
- False start bit detection.
- Complete status reporting capabilities.
- TRI-STATE TTL drive capabilities for bidirectional data bus and control bus.
- Line break generation and detection.
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation.
- Fully prioritized interrupt system controls.

Connection Diagram



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1.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	700 mW

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ±10%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	PC16450C/NS16450		PC8250A/INS8250A		Units
			Min	Max	Min	Max	
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{DD}	2.0	V_{DD}	V
V_{IL}	Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD}	2.0	V_{DD}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all (Note 2)		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0 mA (Note 2)	2.4		2.4		V
I_{CC}(AV)	Avg. Power Supply Current	V_{DD} = 5.5V, T_A = 25°C No Loads on output SIN, DSR, DCD, CTS, RI = 2.4V All other inputs = 0.4V XIN = 8 MHz Divisor = EFFF		10		10	mA
I_{IL}	Input Leakage	V_{DD} = 5.5V, V_{SS} = 0V All other pins floating. V_{IN} = 0V, 5.5V		±10		±10	μA
I_{CL}	Clock Leakage			±10		±10	μA
I_{OZ}	TRI-STATE Leakage	V_{DD} = 5.5V, V_{SS} = 0V V_{OUT} = 0V, 5.5V 1) Chip deselected 2) WRITE mode, chip selected		±20		±20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8		0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		2.0		V

Capacitance T_A = 25°C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	f_c = 1		6	10	pF
C_{OUT}	Output Capacitance	Unmeasured pins returned to V_{SS}		10	20	pF
$C_{I/O}$	Input/Output Capacitance			10	12	pF

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	PC16450C/NS16450		PC8250A/INS8250A		Units
			Min	Max	Min	Max	
t_{ADS}	Address Strobe Width		25		60		ns
t_{AH}	Address Hold Time		0		0		ns
t_{AR}	RD, $\overline{RD}$ Delay from Address	(Note 1)	20		30		ns
t_{AS}	Address Setup Time		25		60		ns
t_{AW}	WR, $\overline{WR}$ Delay from Address	(Note 1)	20		30		ns
t_{CH}	Chip Select Hold Time		0		0		ns
t_{CS}	Chip Select Setup Time		25		60		ns
t_{CSC}	Chip Select Output Delay from Select	@100 pF loading (Note 1)		33		45	ns
t_{CSR}	RD, $\overline{RD}$ Delay from Chip Select	(Note 1)	20		30		ns
t_{CSW}	WR, $\overline{WR}$ Delay from Select	(Note 1)	20		30		ns
t_{DH}	Data Hold Time		10		30		ns
t_{DS}	Data Setup Time		20		30		ns
t_{HZ}	RD, $\overline{RD}$ to Floating Data Delay	@100 pF loading (Note 3)	0	25	0	100	ns
t_{MR}	Master Reset Pulse Width		500		500		ns
t_{RA}	Address Hold Time from RD, $\overline{RD}$	(Note 1)	0		0		ns
t_{RC}	Read Cycle Delay		36		125		ns
t_{RCS}	Chip Select Hold Time from RD, $\overline{RD}$	(Note 1)	0		20		ns
t_{RD}	RD, $\overline{RD}$ Strobe Width		60		125		ns
t_{RDD}	RD, $\overline{RD}$ to Driver Disable Delay	@100 pF loading (Note 3)		20		60	ns
t_{RVD}	Delay from RD, $\overline{RD}$ to Data	@100 pF loading		31		60	ns
t_{WA}	Address Hold Time from WR, $\overline{WR}$	(Note 1)	0		0		ns
t_{WC}	Write Cycle Delay		36		150		ns
t_{WCS}	Chip Select Hold Time from WR, $\overline{WR}$	(Note 1)	0		0		ns
t_{WR}	WR, $\overline{WR}$ Strobe Width		60		100		ns
t_{XH}	Duration of Clock High Pulse	External Clock (8.0 MHz Max.)	55		55		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (8.0 MHz Max.)	55		55		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		115		280		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		115		280		ns
Baud Generator							
N	Baud Divisor		1	$2^{16}-1$	1	$2^{16}-1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		175		175	ns
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		175		175	ns
t_{HW}	Baud Output Up Time	$f_X = 8.0$ MHz, ÷2, 100 pF Load	100		100		ns
t_{LW}	Baud Output Down Time	$f_X = 8.0$ MHz, ÷2, 100 pF Load	100		100		ns
Receiver							
t_{RINT}	Delay from RD, $\overline{RD}$ (RD RBR or RD LSR) to Reset Interrupt	100 pF Load		40		1000	ns
t_{SCD}	Delay from RCLK to Sample Time			33		2000	ns
t_{SINT}	Delay from Stop to Set Interrupt			2		1	RCLK Cycles (Note 2)

Note 1: Applicable only when $\overline{ADS}$ is tied low.

Note 2: RCLK is equal to t_{XH} and t_{XL}.

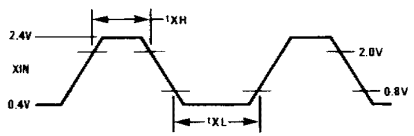
Note 3: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	PC16450C/NS16450		PC8250A/INS8250A		Units
			Min	Max	Min	Max	
Transmitter							
t_{HR}	Delay from WR, $\overline{WR}$ (WR THR) to Reset Interrupt	100 pF Load		40		175	ns
t_{IR}	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF Load		40		250	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	24	16	24	BAUDOUT Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)			8		8	BAUDOUT Cycles
Modem Control							
t_{MDO}	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF Load		40		200	ns
t_{RIM}	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF Load		78		250	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		40		250	ns

4.0 Timing Waveforms (All timings are referenced to valid 0 and valid 1)

External Clock Input (24 MHz Max.)



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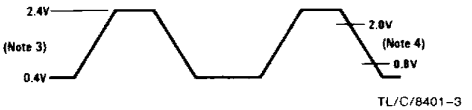
AC Test Points



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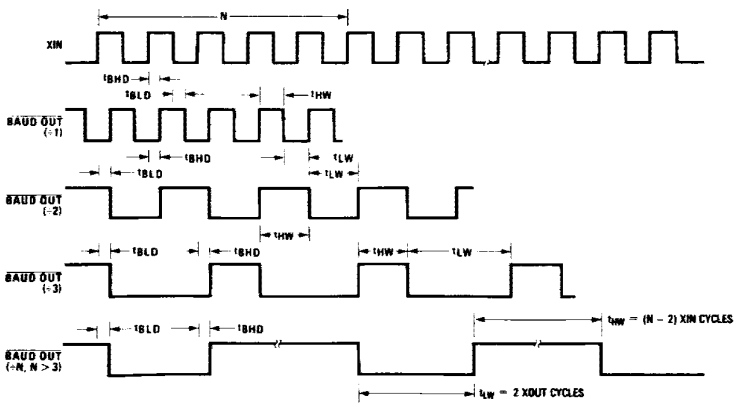
Note 3: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

Note 4: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

$\overline{BAUDOUT}$ Timing



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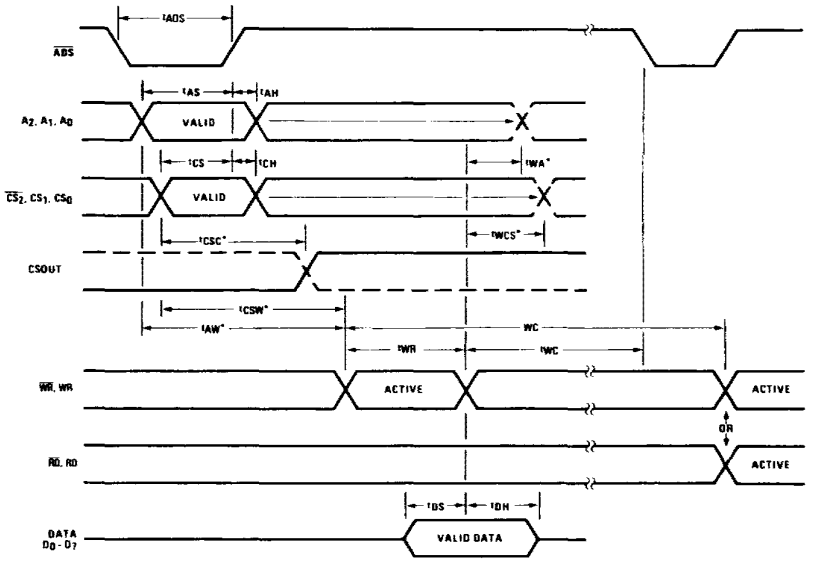
4.0 Timing Waveforms (Continued)

Write Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low.

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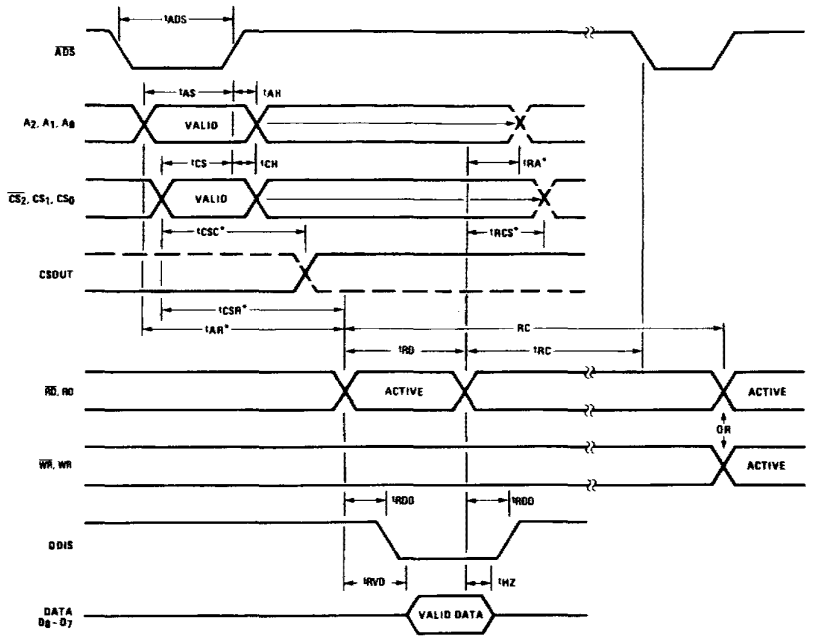
Read Cycle



*Applicable Only When $\overline{ADS}$ is Tied Low.

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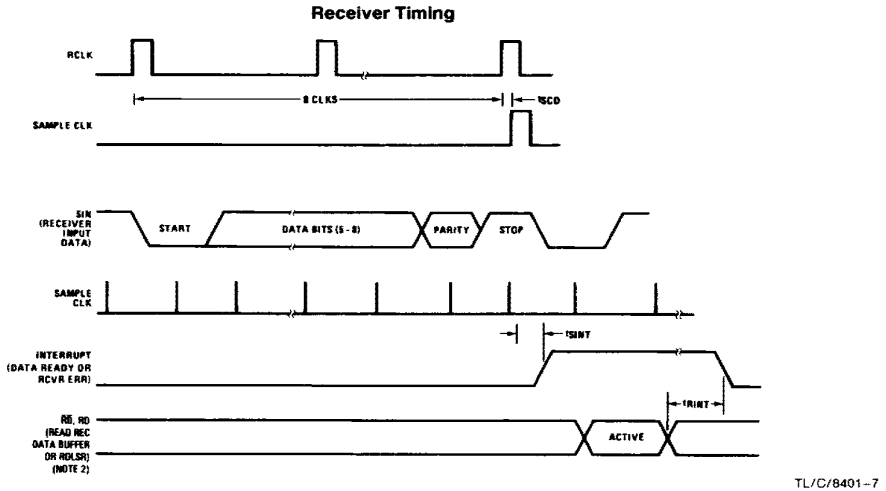
4.0 Timing Waveforms (Continued)

Receiver Timing



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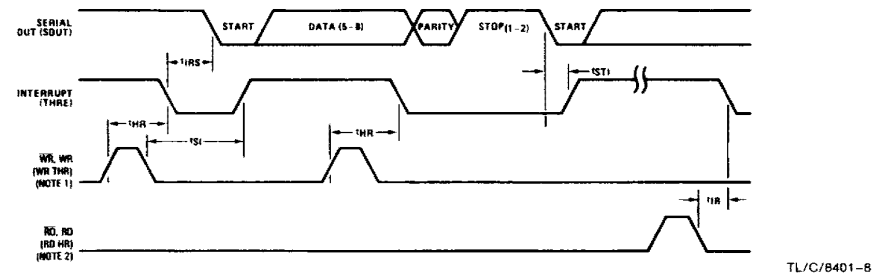
Transmitter Timing



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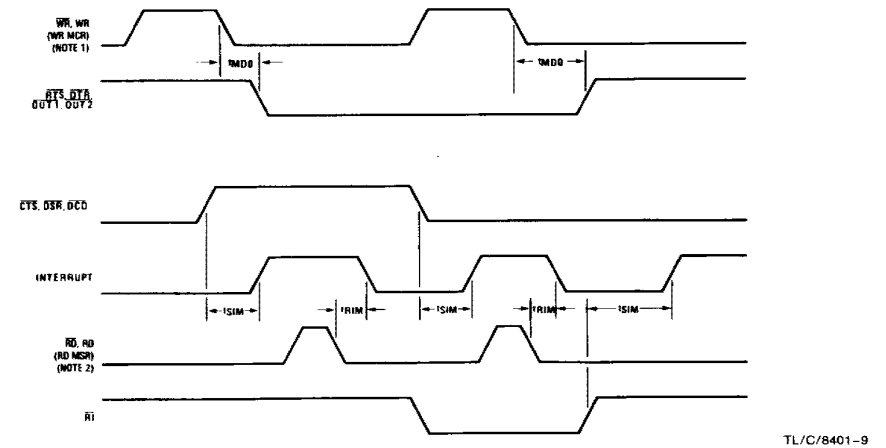
MODEM Controls Timing



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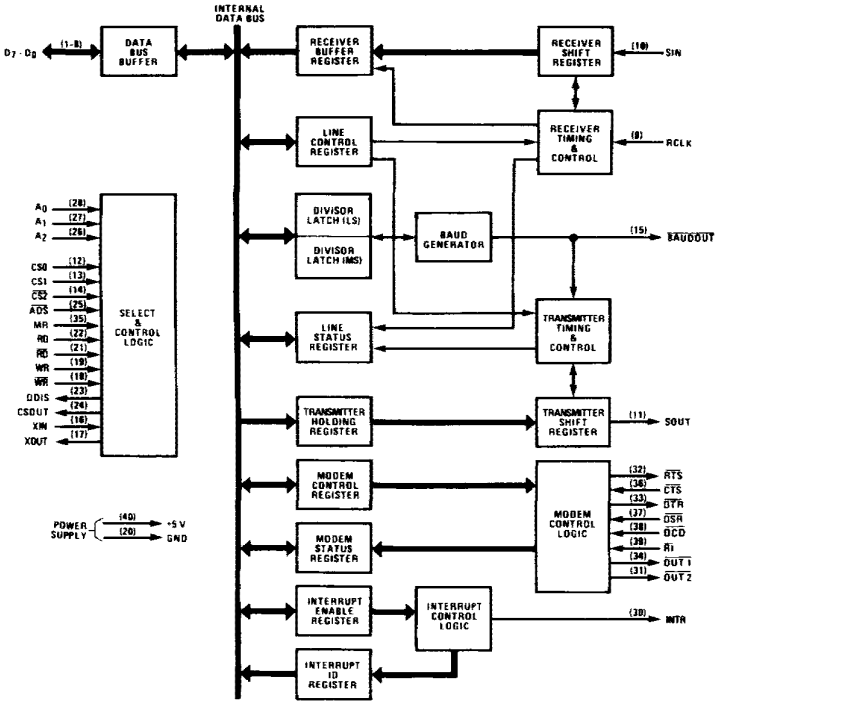
Note 1: See Write Cycle Timing

Note 2: See Read Cycle Timing

5.0 Block Diagram



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Note: Applicable pinout numbers are included within parenthesis.

6.0 Pin Descriptions

The following describes the function of all UART pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

A0, A1, A2: Register Select Pins 26–28: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. The Register Addresses table associates these address inputs with the register they select. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

$\overline{\text{ADS}}$: Address Strobe Pin 25: The positive edge of an active Address Strobe ($\overline{\text{ADS}}$) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active $\overline{\text{ADS}}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{\text{ADS}}$ input permanently low.

$\overline{\text{BAUDOUT}}$: Baud Out Pin 15: This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{\text{BAUDOUT}}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Register Addresses

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)